

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/042924

Filing Date: January 9, 2002

Title: P-CHANNEL DYNAMIC FLASH MEMORY CELLS WITH ULTRATHIN TUNNEL OXIDES

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Dkt: 303.684US2IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method comprising: forming an enhancement mode p-channel memory cell, including:
forming an oxide layer of less than 40 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;
forming a floating gate on and contacting the oxide layer;
forming a dielectric layer on the floating gate; and
forming a control gate on the dielectric layer, wherein the enhancement mode p-channel memory cell is adapted to erase using a potential of magnitude of about 3 V or less applied to the floating gate.

2. (Original) The method of claim 1, wherein forming the oxide layer includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

3. (Original) The method of claim 1, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 10 hours at 20 degrees Celsius.

4. (Original) The method of claim 1, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge of the order of 10^{-17} Coulombs for at least 1.0 second at 85 degrees Celsius.

5. (Original) The method of claim 1, wherein forming the floating gate includes forming a floating gate which has a bottom surface area in contact with the oxide layer of approximately 10^{-10} cm^2 .

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6. (Original) The method of claim 1, wherein forming the p-channel memory cell includes forming the p-channel memory cell to operate at a voltage of approximately 1.0 Volts applied to the control gate.

7.-20. Cancelled.

21. (Currently Amended) A method comprising: forming an enhancement mode p-channel transistor, including:

forming an oxide layer of approximately 23 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;

forming a floating gate on and contacting the oxide layer

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

22. (Original) The method of claim 21, wherein forming a floating gate on the oxide layer includes forming a p-type polysilicon floating gate.

23. (Original) The method of claim 21, wherein forming a floating gate on the oxide layer includes forming a p-type polysilicon-germanium floating gate.

24. (Currently Amended) A method comprising: forming an enhancement mode p-channel memory cell, including:

forming an oxide layer of less than 40 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;

forming a floating gate on and contacting the oxide layer;

forming a dielectric layer on the floating gate; and

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forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel includes forming the enhancement mode p-channel adapted to have a reliability of an number of cycles of performance of approximately 10^{15} cycles over a lifetime of the enhancement mode p-channel memory cell and forming the enhancement mode p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

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cont.*

11. **10**
~~25.~~ (Original) The method of claim ~~24~~, wherein forming a dielectric layer on the floating gate includes forming a layer of silicon dioxide.

12. **10**
~~26.~~ (Original) The method of claim ~~24~~, wherein forming a dielectric layer on the floating gate includes forming a layer of silicon nitride.

13.
~~27.~~ (Currently Amended) A method comprising: forming an enhancement mode p-channel memory cell, including:

forming an oxide layer of less than 40 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;

forming a floating gate on and contacting the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel includes forming the enhancement mode p-channel adapted to have a reliability of an number of cycles of performance of approximately 10^{12} cycles over a lifetime of the enhancement mode p-channel memory cell and forming the enhancement mode p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

14. **13**
~~28.~~ (Original) The method of claim ~~27~~, wherein forming a floating gate on the oxide layer includes forming a heavily doped n-type polysilicon floating gate.

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15. ~~29.~~ (Original) The method of ¹³ ~~27~~, wherein forming a floating gate on the oxide layer includes forming a floating gate which has a bottom surface area in contact with the oxide layer of approximately 10^{-10} cm².

16. ~~30.~~ (Currently Amended) A method comprising: forming an enhancement mode p-channel memory cell, including:

forming an oxide layer of about 30 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;

forming a floating gate on and contacting the oxide layer;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p-channel transistor to have an operating voltage of about 3.0 Volts across the oxide layer.

17. ~~31.~~ (Original) The method of ~~30~~, wherein forming a floating gate on the oxide layer includes forming a floating gate which has a bottom surface area in contact with the oxide layer of approximately 10^{-10} cm².

18. ~~32.~~ (Original) The method of claim ~~30~~, wherein forming a floating gate on the oxide layer includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius.

19. ~~33.~~ (Currently Amended) A method comprising: forming a memory device, including: forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one p-channel memory cell, and wherein forming at least one p-channel memory cell includes:

forming an oxide layer of about 23 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;

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forming a floating gate on and contacting the oxide layer
forming a dielectric layer on the floating gate; and
forming a control gate on the dielectric layer, wherein forming the enhancement mode p-channel transistor includes forming the enhancement mode p-channel transistor to have an operating voltage of approximately 1.0 Volts applied to the control gate; and
forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells.

20.

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~~34.~~ (Original) The method of claim ~~23~~, wherein forming a floating gate on the oxide layer includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius.

21.

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~~35.~~ (Original) The method of claim ~~25~~, wherein forming a floating gate on the oxide layer includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for at least one second at 85 degrees Celsius.

22.

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~~36.~~ (Currently Amended) A method comprising: forming an enhancement mode p-channel transistor, including:

forming an oxide layer of less than 40 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate;

forming a floating gate on and contacting the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-7} 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius;

forming a dielectric layer on the floating gate, the dielectric layer including silicon dioxide; and

forming a control gate on the dielectric layer.

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23. ~~37.~~ (Previously Presented) The method of claim ~~36~~, wherein forming an oxide layer of less than 50 Angstroms (Å) includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

24. ~~38.~~ (Currently Amended) The method of claim ~~36~~, wherein forming the floating gate further includes forming a floating gate which is adapted to hold a charge on the order of 10^{-7} 10^{-17} Coulombs for at least 1.0 second at 85 degrees Celsius.

25. ~~39.~~ (Currently Amended) The method of claim ~~36~~, wherein forming the p-channel transistor further includes forming an ~~intergate dielectric on the floating gate and forming a control gate on the intergate dielectric~~ the source region as a p+ source region.

26. ~~40.~~ (Previously Presented) The method of claim ~~36~~, wherein forming the p-channel transistor includes forming the p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

27. ~~41.~~ (Currently Amended) A method comprising: forming a memory device, including: forming a plurality of memory cells, wherein forming the plurality of memory cells includes forming at least one p-channel memory cell, and wherein forming at least one p-channel memory cell includes:

forming an oxide layer of less than 40 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate; and

forming a floating gate on and contacting the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for longer than 1.0 hour at 20 degrees Celsius.;

forming a dielectric layer on the floating gate; and

forming a control gate on the dielectric layer; and

forming at least one sense amplifier, wherein forming at least one sense amplifier includes coupling the at least one amplifier to the plurality of memory cells.

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28. *27*
~~42.~~ (Previously Presented) The method of claim ~~41~~, wherein forming an oxide layer of less than 50 Angstroms (Å) includes forming the oxide layer to have a thickness of 23 Angstroms (Å).

29. *27*
~~43.~~ (Previously Presented) The method of claim ~~41~~, wherein forming the floating gate further includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for at least 1.0 second at 85 degrees Celsius.

30. *27*
~~44.~~ (Currently Amended) The method of claim ~~41~~, wherein forming the p-channel transistor further includes ~~an intergate dielectric on the floating gate and forming a control gate on the intergate dielectric~~ the source region as a p+ source region.

31. *30*
~~45.~~ (Previously Presented) The method of claim ~~44~~, wherein forming the p-channel transistor further includes forming the p-channel transistor to have an operating voltage of approximately 1.0 Volt on the control gate.

32. *27*
~~46.~~ (Previously Presented) The method of claim ~~41~~, wherein forming the p-channel transistor includes forming the p-channel transistor to have an operating voltage of less than 2.5 Volts across the oxide layer.

33. *27*
~~47.~~ (Currently Amended) A method comprising: forming an enhancement mode p-channel transistor, including:

forming an oxide layer of approximately 23 Angstroms (Å) on and contacting a substrate and contacting a source region, a drain region, and a channel region, the having a channel region separating a the source and a the drain region in the substrate; and

forming a floating gate on and contacting the oxide layer, wherein forming the floating gate includes forming a floating gate which is adapted to hold a charge on the order of 10^{-17} Coulombs for at least one second at 85 degrees Celsius;

forming a dielectric layer on the floating gate; and
forming a control gate on the dielectric layer.

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48. (Previously Presented) The method of claim 47, further including forming a heavily doped p-type source region and a heavily doped p-type drain region.

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49. (Previously Presented) The method of claim 48, wherein forming a heavily doped p-type source region and a heavily doped p-type drain region includes forming the heavily doped p-type source region and the heavily doped p-type drain region in a n-type well.

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